Microsemi

LX8819

Dual Channel 1A Low Dropout Regulator

DATA SHEET

DESCRIPTION

The LX8819 is a dual channel positive-voltage linear regulator. This dual regulator has one fixed output coupled with an adjustable output. Each channel features a low dropout and a high accuracy.

The LX8819 provides designers with a flexible power management solution, minimal printed circuit board area, and shorter design cycles.

Each channel can supply up to one amp independently with a regulator design optimized for system efficiency by consuming minimal ground current while directing quiescent current to the load.

The LX8819 features on-chip trimming of the internal voltage reference enabling precise output Voltages (typically ±1% of its specified value) while the Bipolar output transistor has a low dropout voltage even at full output current (V_{DO} < 1.25V typical @ 1A).

Thermal and Short Circuit Current Protection are integrated on-chip and operate independently for each of the regulator output.

The LX8819 regulator is stable with a low-value output capacitor (typically 2.2µF on the outputs) allowing the designers flexibility in external component selection.

Microsemi's S-PAK and D-PAK power packages enable maximum power dissipation and ease of assembly using surface mount technology.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

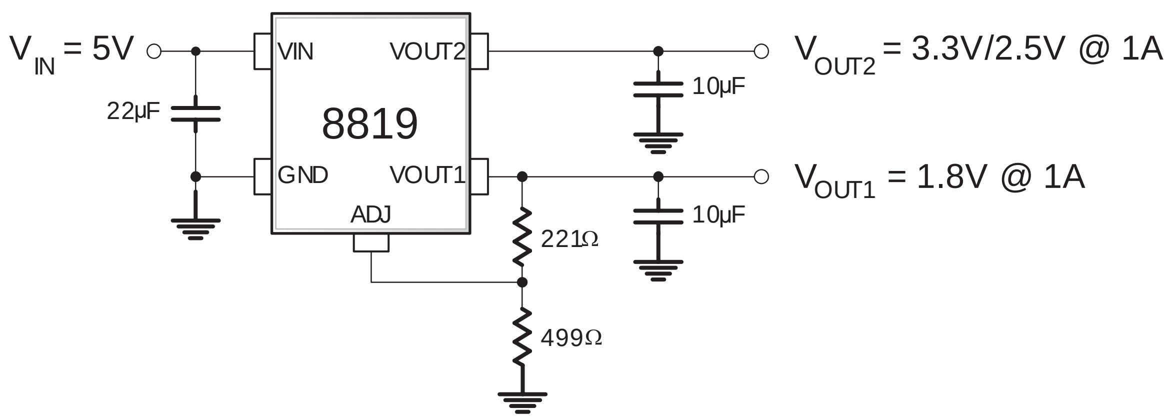
KEY FEATURES

- Two Independent Regulated Outputs
- Accurate Output Voltages
- Typical Dropout of 1.25V at 1A and 1.1V at 500mA
- Independent Thermal and Current Limit Protection
- Low Profile 5 Lead SMT Power Package
- Low Tolerance Load Regulation
- Wide DC Supply Voltage of 3.5V to 10V
- Loop Stability Independent of Output Capacitor Type

APPLICATIONS

- 5V to 3.3V / ADJ Regulators
- Hard Disk Drives, CD-ROMs
- ADSL and Cable Modems
- Battery Charging Circuits
- Instrumentation
- PC Peripherals

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_J (°C)	Output V_1 (Pin 4)	Output V_2 (Pin 5)	DF Plastic S-PAK 5 pin RoHS Compliant Transition DC: 0515	DT Plastic D-PAK 5-Pin
0 to 125	Adj.	3.3	LX8819-33CDF	LX8819-33CDT
	Adj.	2.5	LX8819-25CDF	LX8819-25CDT

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX8819-33CDT-TR)

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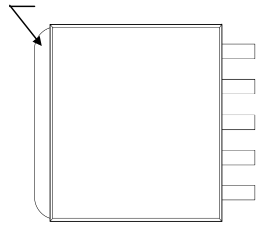
ABSOLUTE MAXIMUM RATINGS

Input Voltage (VIN)..13.5V
Load Current (Internally Limited) 1A
Power Dissipation ....Internally Limited
Short-Circuit Protection .... Indefinite
Operating Temperature Range .... 0°C to 150°C
Maximum Operating Junction Temperature .... 150°C
Storage Temperature Range..-65°C to 150°C
Lead Temperature (Soldering 180 seconds) .... 235°C
RoHS Peak Package Solder Reflow Temperature
(40 second maximum exposure) .... 260°C (+0, -5)

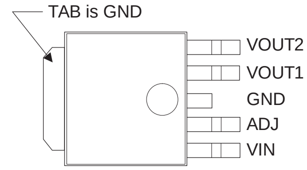
Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



DF PACKAGE
(Top View)

RoHS 100% Matte Tin Lead Finish



DT PACKAGE
(Top View)

THERMAL DATA

DF **Plastic S-PAK 5-Pin**

THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	5°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	30°C/W

DT **Plastic D-PAK 5-Pin**

THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	6°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	32°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.
θ_{JA} can vary from 25°C/W to > 40°C/W depending on mounting technique. (See Application Notes Section: Thermal considerations)

FUNCTIONAL PIN DESCRIPTION

Name	Description
VIN	Positive unregulated supply input for the regulator – Bypass to GND with at least 2.2µF capacitance having low ESR for good transient response.
ADJ	Adjustable regulator feedback input – The output voltage can be set by two external resistors with the following relationship: $VOUT1 = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$ where R_1 is the resistor connected between VOUT1 and ADJ, and R_2 is the resistor connected between ADJ and GND.
GND	Common terminal for ground reference – The input and output bypass capacitors should be connected to this pin. In addition the tab on the S-Pak package and pin 3 are also used for heat sinking the device.
VOUT1	Adjustable regulator output (Regulator #1) – It is recommended to bypass to GND with at least 2.2µF. Size your output capacitor to meet the transient loading requirement. If you have a very dynamic load, a lower ESR capacitor will improve the response to these load steps.
VOUT2	Fixed regulator output (Regulator #2) – It is recommended to bypass to GND with at least 2.2µF. Size your output capacitor to meet the transient loading requirement. For dynamic loads, a lower ESR capacitor will improve the response to these load steps.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	LX8819			Units
		Min	Typ	Max	
Input Voltage - 3.3V	V_{IN}	4.5		10	V
Input Voltage - 2.5V < 200mA Load		3.5		10	V
Output Voltage (Adjustable)	V_{OUT}			5	V
Load Current (Each Output)[1]	I_{OUT}	0		1000	mA
Input Capacitor (VIN to GND)	C_{IN}	2.2	20		µF
Output Capacitor (VOUTx to GND)[2]	C_{OUT}	1.0	10		µF

Note 1: Care should be taken so as to not exceed the thermal dissipation capability of the package
2: Size your output capacitor to meet the transient loading requirement. If you have a very dynamic load, a lower ESR and larger value capacitor will improve the response to these load steps.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ TA ≤ 125°C except where otherwise noted and with the following test conditions: V_{IN} = 5V, I_{OUT} = 10mA, C_{IN}= 10µF (Tantalum), C_{OUT} = 4.7µF (Tant.), and $T_J = T_A$ using low duty cycling methods.

Parameter	Symbol	Test Conditions	LX8819			Units
			Min	Typ	Max	
ADJUSTABLE OUTPUT (VOUT1)						
Reference Voltage	V_{REF}	5mA < I_{OUT1} < 1A, 4.75V < V_{IN} < 5.5V	1.225	1.25	1.275	V
Line Regulation	$\Delta V_{REF}(V_{IN})$	3.75V < V_{IN} < 5.5V, I_{OUT1} = 5mA		1.5	6	mV
Load Regulation	$\Delta V_{REF}(I_{OUT})$	5mA < I_{OUT1} < 1A, V_{IN} = 4.75V		0.18	0.36	$\%V_{OUT}$
Dropout Voltage	ΔV	I_{OUT1} = 1A, ΔV_1 = -1%		1.3	1.46	V
Current Limit	$I_{OUT\ (MAX)}$		1.0	1.4		A
Minimum Load Current	I_L	Note 3		2	3	mA
Adjust Pin Bias Current	I_{ADJ}			-0.12	-1	µA
FIXED OUTPUT (OUTPUT 2)						
Output Voltage – LX8819-33	V_{OUT}	5mA < I_{OUT2} < 1A, 4.75V < V_{IN} < 5.5V	3.217	3.30	3.383	V
Output Voltage – LX8819-25		5mA < I_{OUT2} < 0.2A, 3.75V < V_{IN} < 5.5V	2.437	2.5	2.562	
Line Regulation	$\Delta V_{OUT}(V_{IN})$	4.75V < V_{IN} < 5.5V, I_{OUT2} = 5mA		6	8	mV
Load Regulation	$\Delta V_{OUT}(I_{OUT})$	5mA < I_{OUT2} < 1A, V_{IN} = 4.75V		6	12	mV
Dropout Voltage	ΔV	I_{OUT2} = 1A, $\Delta V2$ = -1%		1.25	1.41	V
		I_{OUT2} = 0.2A, $\Delta V2$ = -1%			1.25	V
Current Limit	$I_{OUT\ (MAX)}$		1.0	1.4		A
Minimum Load Current	I_{OUT}				0	mA
ENTIRE REGULATOR						
Quiescent Current	I_Q	V_{IN} < 5.5V, I_{OUT1} = 5mA, I_{OUT2} = 5mA		2.6	4.2	mA
		$V_{IN} \leq$ 5.5V, I_{OUT1} = 1A, I_{OUT2} = 1A		3.5	5	
VIN Under Voltage Lockout Threshold	UVLO	-3.3 Voltage Rising	2.5		4.5	V
		-2.5 Voltage Rising @ 25 °C	2.5		3.6	
V_{OUT} Rise Time for VIN Switched On	$V_{OUT}(t_R)$		80		300	µs
Ripple Rejection	PSRR	f=120Hz, V_{IN} = 5V	60	75		dB
RMS Output Noise	$V_{OUT\ (RMS)}$	10Hz < f < 10kHz		0.003		$\%V_{OUT}$
Thermal Shutdown	T_{JSD}		150	165		°C

Note 3: Minimum load current is defined as the amount of output current required to maintain regulation. , The external resistor divider current can be included in this requirement.

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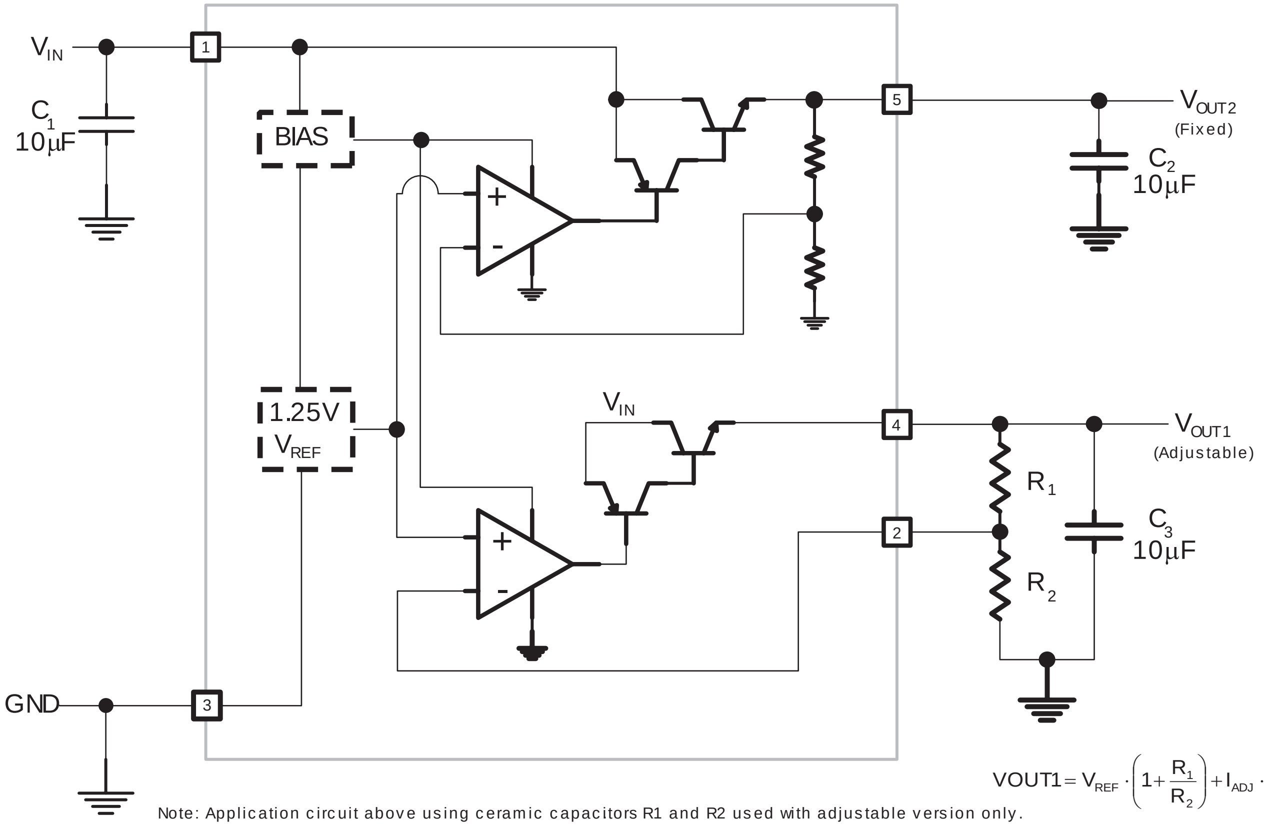
SIMPLIFIED BLOCK DIAGRAM



$$VOUT1 = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$$

Note: Application circuit above using ceramic capacitors R1 and R2 used with adjustable version only.

Figure 1 – Simplified Block Diagram

APPLICATION INFORMATION

DESCRIPTION

The LX8819 is part of a family of Dual LDO (Low Drop-Out) linear regulators in Microsemi's S-PAK power package which offer maximum power dissipation in a low profile surface mount technology. The family includes a combination of fixed and adjustable versions. Each channel can supply up to one amp independently with a regulator design optimized for system efficiency by consuming minimal ground current and directing quiescent current to the load.

INPUT CAPACITOR

To improve load transient response and noise rejection an input bypass capacitor of at least 2.2µF is required. Generally it is recommended that a 20µF ceramic/tantalum or 22µF electrolytic capacitor be used.

OUTPUT CAPACITOR

The LX8819 regulator requires output capacitors connected between each voltage output and ground to stabilize the internal control loop. Many types of capacitors, with different capacitance values, tolerances, temperature coefficients, and equivalent series resistance are available for use with the LX8819. It is recommended that a minimum of 4.7µF be used at each voltage output.

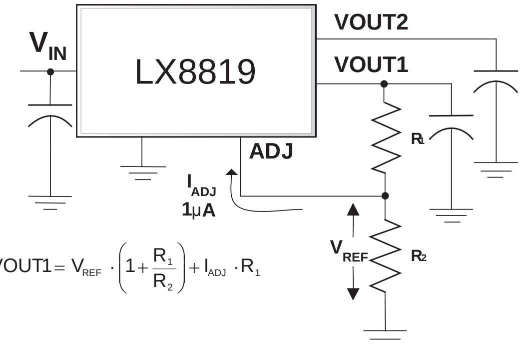
To ensure good transient response from the power supply system under rapidly changing current load conditions, designers generally use additional output capacitors connected in parallel. Such an arrangement serves to minimize the effects of the parasitic resistance (ESR) and inductance (ESL) that are present in all capacitors. The regulator has been tested stable with capacitor ESR's in the range of 50mΩ to 2Ω. It is generally best to use the same type of capacitors for both input and output bypassing.

ADJUSTABLE OUTPUT VOLTAGE

The LX8819 develops a 1.25V reference voltage between the adjust terminal and ground (See Figure 2). By placing a resistor, R_2, between these two terminals, a constant current is caused to flow through R_1 and down through R_2 to set the overall output voltage. Because I_{ADJ} is very small and constant when compared with the current through R_2, it represents a small error and can usually be ignored.

MINIMUM LOAD REQUIREMENT

The LX8819 has a minimum load requirement for proper output regulation. This minimum current is specified at 0mA for the fixed output and 2mA for the adjustable output regulator.



$$VOUT1 = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$$

Figure 2 – Basic Regulator Circuit

TEMPERATURE PROTECTION

The thermal protection shuts the LX8819 down when the junction temperature exceeds 140°C. Each output has independent thermal shutdown capability. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (See Thermal Considerations below).

CURRENT LIMIT PROTECTION

The LX8819 includes over current protection. When the output load current exceeds 1.4A (typical) the current limit protection circuit forces the regulator to decrease the output current in order to maintain safe levels.

THERMAL CONSIDERATIONS

Thermal shutdown protection circuitry protects the integrated circuit from thermal overload caused from a rise in junction temperature during excessive power dissipation conditions. This means of protection is intended for fault protection only and not as a means of current or power limiting during normal application usage.

Proper thermal evaluation should be done to ensure that the junction temperature (T_J) does not exceed its maximum rating. Continuous operation at the maximum T_J of 150°C can impact reliability.

Due to variation in individual device electrical characteristics and thermal resistance, the built in thermal overload protection may be activated at power levels slightly above or below the rated dissipation. Also, peak output power should be considered for each individual output.

Total power dissipation for the regulator can be calculated using the following equation:

$$P_D = \left(V_{IN(MAX)} - V_{OUT1}\right) \cdot I_{OUT1} + \left(V_{IN(MAX)} - V_{OUT2}\right) \cdot I_{OUT2}$$

(Note: Power dissipation resulting from quiescent (ground) current is negligible and ignored)

APPLICATION INFORMATION

Using the calculated total power dissipation, the maximum junction temperature can be calculated using the given temperature coefficients (See Thermal Data) for the selected package.

THERMAL CALCULATION EXAMPLE

Given the following application parameters:

$$T_A = 50°C$$

$$V_{IN(MAX)} = 5V + 5\%$$

$$V_{OUT1} = 1.5V$$

$$V_{OUT2} = 2.5V$$

$$I_{OUT1(MAX)} = I_{OUT2(MAX)} = 500mA$$

The maximum junction temperature of the LX8819 can be calculated using the following equation:

$$T_J = T_A + \left(P_{D(REG1)} + P_{REG2}\right) \cdot \theta_{JA}$$

with:

$$P_{D(REG1)} = \left(V_{IN(MAX)} - V_{OUT1}\right) \cdot I_{OUT1}$$

and

$$P_{D(REG2)} = \left(V_{IN(MAX)} - V_{OUT2}\right) \cdot I_{OUT2}$$

Substituting the known values yields a maximum junction temperature of:

$$P_{D(REG1)} = (5.25V - 1.5V) \cdot 0.5A = 1.75W$$

$$P_{D(REG2)} = (5.25V - 2.5V) \cdot 0.5A = 1.375W$$

$$T_J = T_A + \left(P_{D(REG1)} + P_{D(REG2)}\right) \cdot \theta_{JA}$$

$$T_J = 50°C + (1.75W + 1.375W) \cdot 30 \frac{°C}{W}$$

$$T_J = 140°C$$

This value is within the safe operating range of the device under worst case conditions

It is important to note that although each output of the regulator will produce up to 1A in current, the individual or total power dissipation may limit the useful total current draw. The junction temperature should be calculated for each individual output as well as the combined outputs to insure that maximum junction temperature in not exceeded.

LAYOUT CONSIDERATION

The layout must be done with low impedance paths for VIN, VOUT1, VOUT2 and GND by using sufficiently wide traces to avoid voltage drops and noise pick up. The output capacitors must be placed as close as possible to the voltage regulator output pins.

The input capacitor should be connected between VIN and the ground plane with short leads.

Although it may not be immediately obvious, best load regulation for the adjustable output is obtained when the top of the voltage feedback resistor divider (R_1) is connected as close as possible to the case of the regulator; not to the load.

The PCB copper can be used as a heatsink for the surface mounted package. Using the minimum size as shown in the recommended pad layout (Figure 3), limits the usable power to about 1W for an ambient temperature of 50°C. Since most applications require greater than 2W there is the need to provide additional heatsinking. This can be accomplished by using additional copper area both on the PCB surface, as shown in the possible heat sink layout below, or to an embedded ground plane. Since the die pad (copper tab) is in electrical contact with ground, the designer can use thermal vias, on the surface of the PCB, taking advantage of the heat-spreading (Cu) layer of an internal ground plane.

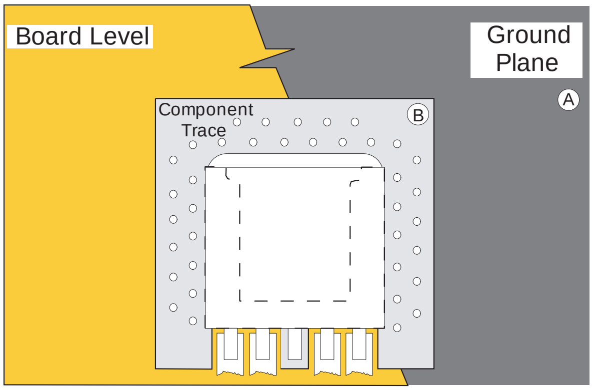


Figure 3 – Recommended Layout

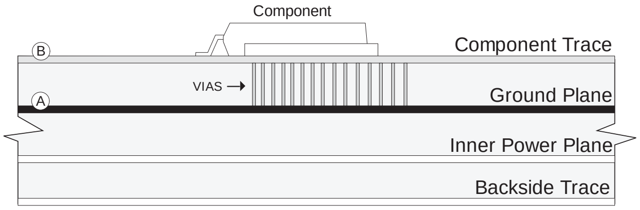


Figure 4 – Ground Plane Heatsink

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APPLICATIONS

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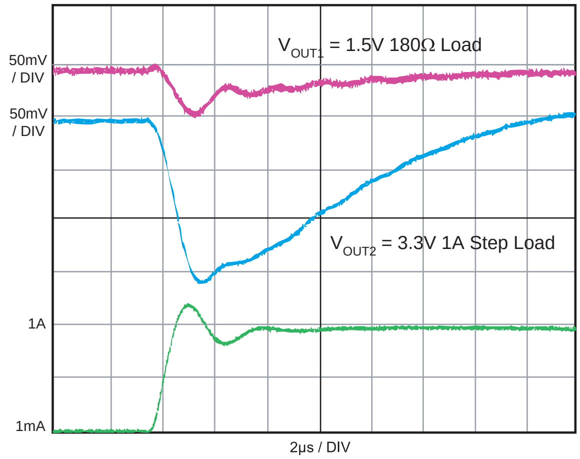
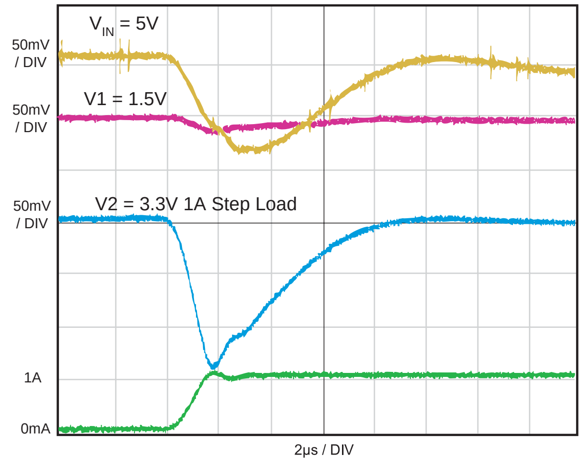
TRANSIENT RESPONSE-CERAMIC CAP



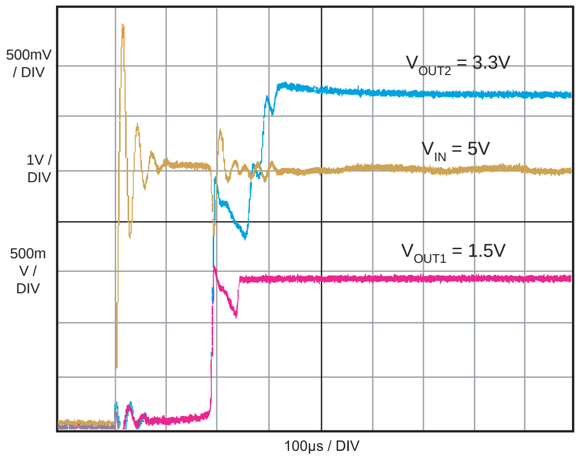
C_{IN} = 20µF Ceramic (ESR= 45mΩ)
COUT(VOUT1) = COUT(VOUT2) = 10µF Ceramic (ESR= 75mΩ)

TRANSIENT RESPONSE-TANT CAP

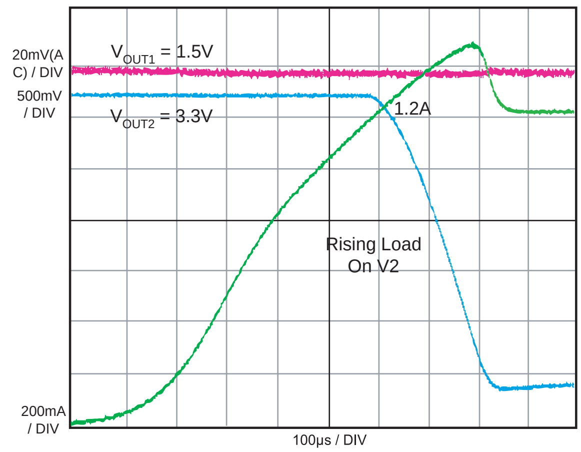


C_{IN} = 22µF Tantalum (ESR= 232mΩ)
$C_{OUT(VOUT1)}$ = $C_{OUT(VOUT2)}$ = 10µF Tantalum (ESR= 198mΩ)

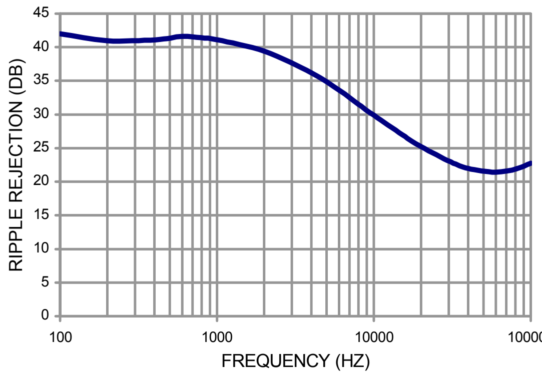
TURN ON CHARACTERISTICS



CURRENT LIMIT



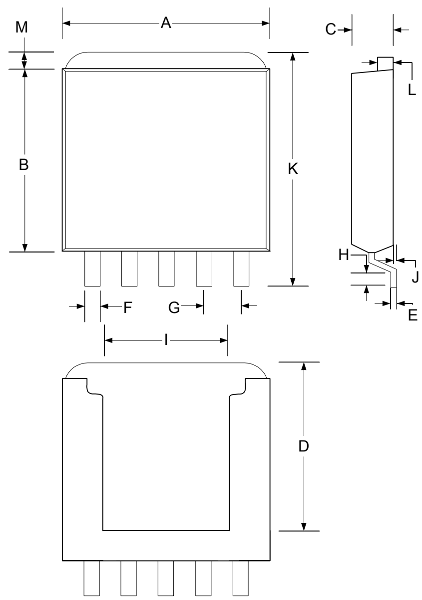
RIPPLE REJECTION



V_{IN} = 5V, C_{IN} = 22µF, $C_{OUT1,2}$ = 10µF, V_{OUT2}=3.3V, I_{OUT2}=1A

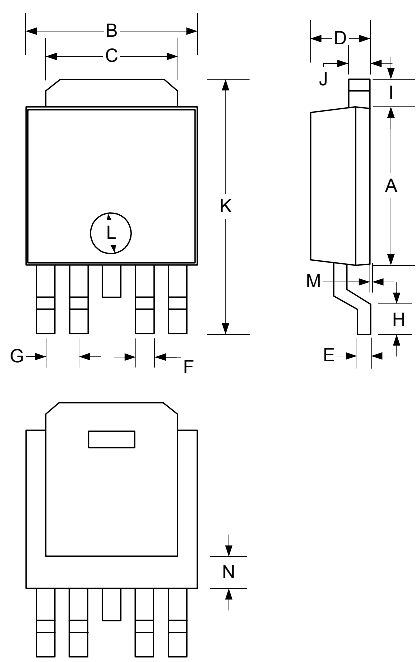
PACKAGE DIMENSIONS

DF 5-Pin S-PAK



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.27	9.52	0.365	0.375
B	7.87	8.13	0.310	0.320
C	1.78	2.03	0.070	0.080
D	2.80	3.10	0.110	0.122
E	1.50	1.75	0.059	0.069
F	0.63	0.79	0.025	0.031
G	1.70 BSC		0.067 BSC	
H	0.79	1.04	0.031	0.041
I	6.50 BSC		0.256 BSC	
J	0.03	0.13	0.001	0.005
K	10.41	10.67	0.410	0.420
L	0.76	1.27	0.030	0.050

DT 5-Pin TO-252 (D-PAK)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.96	6.22	0.234	0.244
B	6.47	6.73	0.254	0.264
C	5.00	5.22	0.196	0.205
D	2.18	2.38	0.085	0.093
E	0.45	0.55	0.017	0.021
F	0.63	0.78	0.024	0.030
G	1.27 BSC		0.050 BSC	
H	1.08	1.29	0.042	0.050
I	1.01	1.11	0.039	0.043
J	0.76	0.86	0.029	0.033
K	9.70	10.08	0.381	0.396
L	1.52	1.62	0.059	0.063
M	0.03	0.13	0.001	0.005
N	1.27 REF		.05 REF	

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES